REMARKS

Claims 1-20 are pending in the current application. Claim 18 has been amended. Applicant thanks the Examiner for the indication that dependent claims 2, 6, 9, 10, 16, and 17 would be allowable if rewritten in independent form. The outstanding issues are:

- Claims 1, 3-5, 7, 8, 11-15, and 18-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Poimboeuf et al. (U.S. Patent No. 6,067,411, hereinafter *Poimboeuf*;

- Claims 1, 11, 15, 18, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hart et al. (U.S. Patent No. 5,721,689, hereinafter *Hart*); and

- Claims 3-5, 7, 8, 12-14, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hart* in view of *Poimboeuf*.

In response, Applicant respectfully traverses the outstanding rejections, and requests reconsideration and withdrawal in light of the remarks presented herein.

I.   Claim Amendments

Claim 18 has been amended to correct inadvertent errors by deleting the term "provided by said means for providing," and to correct the terms "means for cyclically counting" and "integer number of sample intervals." Accordingly, no new matter is presented. Moreover, these corrections are not intended to narrow the scope of the claim.

II.   Rejections Under § 102(b)

Claims 1, 3-5, 7, 8, 11-15, and 18-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Poimboeuf*. Office Action, page 2. Applicant traverses the rejection and asserts that the claims are allowable, at least, for the reasons stated below.

In order anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim. *See* M.P.E.P. § 2131. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." M.P.E.P. 2131, citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Moreover, "[T]he identical invention must be shown in as complete detail as is contained in the … claim." M.P.E.P. § 2131, citing *Richardson v.*

Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989). Applicant asserts that the art of record does not teach every element of the claims, and does not show the identical invention in as complete detail as is contained in the claims.

A.   Claims 1, 3-5, 7, and 8

Claim 1 recites, in part, "adjusting a sample rate so that an integer number of sample intervals equals said period of said signal." The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[T]he UST_CLK signal is a nominal 50% duty cycle asynchronously gate dock. The rate of the UST_CLK is set so that there are an integer number of nanoseconds per clock period."
>
> *Poimboeuf*, col. 5, lines 12-25.

Applicant respectfully points out that the above passage does not teach adjusting a sample rate, nor does it teach adjusting a sample rate so that an integer number of sample intervals equals a period of a signal, as required by claim 1. In fact, *Poimboeuf*'s UST_CLK signal is simply a synthesized clock signal that "corresponds to a uniform, monotonically increasing timeline." *Poimboeuf*, col. 4, lines 47-49. Therefore, there is no sampling involved in the synthesis of UST_CLK. No other section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 1 be withdrawn.

Claim 1 also recites, in part, "configuring a cyclic counter to reset according to said integer number." The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[W]ith reference to FIG. **8**, the FIRM (Integer +Reminder/Modulus) frequency synthesizers **840, 842, 844, 846** work on the principle of dividing a reference clock by an integer (I), plus a ratio (R/M), such that there are, on average, precisely I plus R/M input clock cycles per output clock transition."
>
> *Poimboeuf*, col. 14, lines 20-25.

Applicant respectfully points out that the above passage does not teach configuring a cyclic counter, nor does it teach configuring a cyclic counter to reset according to an integer number, as required by claim 1. In fact, *Poimboeuf* simply teaches a set of frequency

synthesizers which perform a frequency division operation on a reference clock signal.
Poimboeuf, col. 14, lines 20-25. This is not the same, or even similar to configuring a cyclic
counter to reset according to an integer number. No other section of *Poimboeuf* teaches the
claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b)
rejection of record with respect to claim 1 be withdrawn.

Claim 1 further recites, in part, "capturing ensembles of data samples of said signal
that are respectively defined by successive resets of said cyclic counter." Applicant
respectfully points out that *Poimboeuf* does not teach capturing ensembles of data samples of
a signal that are respectively defined by successive resets of a cyclic counter, at least, because
it does not teach resetting a cyclic counter, as noted above. No section of *Poimboeuf* teaches
the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b)
rejection of record with respect to claim 1 be withdrawn.

Dependent claims 3-5, 7, and 8 depend either directly or indirectly from claim 1, and
thus inherit all the limitations of that independent claim. As noted above, *Poimboeuf* does
not teach every element of independent claim 1. Consequently, *Poimboeuf* also fails to teach
every element of dependent claims 3-5, 7, and 8. Accordingly, Applicant respectfully
requests that the 35 U.S.C. § 102(b) rejection of record with respect to claims 3-5, 7, and 8 be
withdrawn.

B.   Claims 11-15

Claim 11 recites, in part, "sample capture circuitry for obtaining samples of said
signal at a sample rate such that an integer number of sample intervals equals said period."
The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[T]he FIRM frequency synthesizers **840, 842, 844, 846** are
> programmed by software to have a set of values in registers which are
> easily derived from I,R, M, the FIRM frequency synthesizers **840, 842,
> 844, 846** generate output clock signals whose transitions are quantized
> to the edges of the reference clock, and at a rate equal to
> N/D=1/(I+R/M) times the reference dock rate. To create a output with
> better jitter characteristics, this pulse train can drive a toggle select
> apparatus. The output of this apparatus leads to the final synthesizer
> output."
>
> *Poimboeuf*, col. 14, lines 25-34.

Applicant respectfully points out that *Poimboeuf* does not teach a sample capture circuitry, nor does it teach a sample capture circuitry for obtaining samples of a signal at a sample rate such that an integer number of sample intervals equals a period, as required by claim 11. In fact, there is no sampling involved in the synthesis of *Poimboeuf*'s clock signals. *Poimboeuf*, col. 4, lines 47-49. No other section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 11 be withdrawn.

Claim 11 also recites, in part, "cyclic counter logic that counts each captured sample and comprising a programmable modulus set to said integer number." The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[W]ith reference to FIG. **8**, the FIRM (Integer +Reminder/Modulus) frequency synthesizers **840, 842, 844, 846** work on the principle of dividing a reference clock by an integer (I), plus a ratio (R/M), such that there are, on average, precisely I plus R/M input clock cycles per output clock transition." The FIRM frequency synthesizers **840, 842, 844, 846** are programmed by software to have a set of values in registers which are easily derived from I,R, M, the FIRM frequency synthesizers **840, 842, 844, 846** generate output clock signals whose transitions are quantized to the edges of the reference clock, and at a rate equal to $N/D=1/(I+R/M)$ times the reference dock rate. To create a output with better jitter characteristics, this pulse train can drive a toggle select apparatus. The output of this apparatus leads to the final synthesizer output."
>
> *Poimboeuf*, col. 14, lines 20-34.

Applicant respectfully points out that the above passage does not teach cyclic counter logic, nor does it teach a cyclic counter logic that counts each captured sample and comprises a programmable modulus set to an integer number, as required by claim 11. In fact, *Poimboeuf* simply teaches a set of frequency synthesizers which perform a frequency division operation on a reference clock signal. *Poimboeuf*, col. 14, lines 20-34. This is not the same, or even similar to a cyclic counter logic that counts each captured sample and comprises a programmable modulus set to an integer number. No other section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 11 be withdrawn.

Claim 11 further recites, in part, "sample capture circuitry ... operable to output time aligned ensembles of captured samples that are defined by respective resets of said cyclic counter logic." Applicant respectfully points out that *Poimboeuf* does not teach the recited feature, at least, because it does not teach resetting a cyclic counter logic, as noted above. No section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 1 be withdrawn.

Dependent claims 12-15 depend either directly or indirectly from claim 11, and thus inherit all the limitations of that independent claim. As noted above, *Poimboeuf* does not teach every element of independent claim 11. Consequently, *Poimboeuf* also fails to teach every element of dependent claims 12-15. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claims 12-15 be withdrawn.

C.   Claims 18-20

Claim 18, as amended, recites, in part, "means for providing samples of said signal at a sample rate, wherein an integer number of sample intervals defined by said sample rate equals said period." The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[T]he FIRM frequency synthesizers **840, 842, 844, 846** are programmed by software to have a set of values in registers which are easily derived from I,R, M, the FIRM frequency synthesizers **840, 842, 844, 846** generate output clock signals whose transitions are quantized to the edges of the reference clock, and at a rate equal to N/D=1/(I+R/M) times the reference dock rate. To create a output with better jitter characteristics, this pulse train can drive a toggle select apparatus. The output of this apparatus leads to the final synthesizer output."
>
> *Poimboeuf,* col. 14, lines 25-34.

Applicant respectfully points out that *Poimboeuf* does not teach means for providing samples of said signal at a sample rate, nor does it teach that an integer number of sample intervals defined by said sample rate equals said period, as required by claim 18. In fact, there is no sampling involved in the synthesis of *Poimboeuf*'s clock signals. *Poimboeuf,* col. 4, lines 47-49. No other section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant

respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 18 be withdrawn.

Claim 18, as amended, also recites, in part, "means for cyclically counting samples such that said means for cyclically counting is reset after said integer number." The Examiner relies upon the following passage of *Poimboeuf* as teaching this feature:

> "[W]ith reference to FIG. **8**, the FIRM (Integer +Reminder/Modulus) frequency synthesizers **840, 842, 844, 846** work on the principle of dividing a reference clock by an integer (I), plus a ratio (R/M), such that there are, on average, precisely I plus R/M input clock cycles per output clock transition." The FIRM frequency synthesizers **840, 842, 844, 846** are programmed by software to have a set of values in registers which are easily derived from I,R, M, the FIRM frequency synthesizers **840, 842, 844, 846** generate output clock signals whose transitions are quantized to the edges of the reference clock, and at a rate equal to N/D=1/(I+R/M) times the reference dock rate. To create a output with better jitter characteristics, this pulse train can drive a toggle select apparatus. The output of this apparatus leads to the final synthesizer output."
>
> *Poimboeuf*, col. 14, lines 20-34.

Applicant respectfully points out that the above passage does not teach a means for cyclically counting samples, nor does it teach that the means for cyclically counting be reset after the integer number of sample intervals, as required by claim 18. In fact, *Poimboeuf* simply teaches a set of frequency synthesizers which perform a frequency division operation on a reference clock signal. *Poimboeuf*, col. 14, lines 20-34. This is not the same, or even similar to a means for cyclically counting samples such that the means for cyclically counting is reset after an integer number of sample intervals. No other section of *Poimboeuf* teaches the claimed feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 18 be withdrawn.

Claim 18, as amended, further recites, in part, "means for outputting time aligned ensembles of samples defined by respective resets of said means for cyclically counting." Applicant respectfully points out that *Poimboeuf* does not teach the recited feature, at least, because it does not teach a means for cyclically counting samples that is reset after the integer number of sample intervals, as noted above. No section of *Poimboeuf* teaches the claimed

feature. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claim 18 be withdrawn.

Dependent claims 19 and 20 depend either directly or indirectly from claim 18, and thus inherit all the limitations of that independent claim. As noted above, *Poimboeuf* does not teach every element of independent claim 18. Consequently, *Poimboeuf* also fails to teach every element of dependent claims 19 and 20. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of record with respect to claims 19 and 20 be withdrawn.

III.   Rejections Under § 103(a) over *Hart*

Claims 1, 11, 15, 18, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hart*. Office Action, page 3. Applicant traverses the rejection and asserts that the claims are allowable, at least, for the reasons stated below.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the references' teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See M.P.E.P. § 2143. Applicant respectfully asserts that the rejection does not satisfy the basic criteria.

A.   Lack of Motivation

The Examiner has not advanced any suggestion or motivation for modifying *Hart*, or for combining *Hart* with another reference. In fact, the Examiner simply states that "it would have been obvious to one of ordinary skill in the art to realize that Hart et al.'s operation is [sic] commonly indicates the capturing ensembles of data samples of the signal in order to provide the results for monitoring manner [sic]." Office Action, page 4. However, Applicant points out that the foregoing statement does not identify any suggestion or motivation to modify *Hart*. Therefore, the Examiner has not met the initial burden of factually supporting any *prima facie* conclusion of obviousness. *See* M.P.E.P. § 2142.

Applicant asserts that there is no suggestion or motivation, either in the prior art or the knowledge available to a person of ordinary skill in the art, to modify *Hart*. Accordingly, Applicant respectfully asserts that, for the above reasons, claims 1, 11, 15, 18, and 19 are patentable over the 35 U.S.C. § 103(a) rejection of record.

B.   Lack of All Claimed Limitations

With respect to claim 1, the Examiner admits that *Hart* does not teach or suggest "capturing ensembles of data samples of said signal that are respectively defined by successive resets of said cyclic counter." Office Action, page 4. However, according to the Examiner, the following passage of *Hart* "indicates the capturing ensembles of data samples of the signal in order to provide the results for monitoring manner [sic]" (Office Action, page 4):

> "[A] flowchart of the steps carried out according to this prior frequency tracking procedure is shown in FIG. **4**. The routine obtains a new sample at step **102** and increments a counter at step **104**. A voltage phasor is generated at step **106** using an N-point DFT during each sampling interval. This phasor is also compared with a reference phasor to obtain the angle [theta] at step **106**. If the frequency has drifted a sufficient amount, [theta] will be larger than a preset limit, LIMIT1, as determined at step **108**. According to this technique, [theta] is the angle between the reference phasor and the latest phasor estimate and is specified by M*N times the consecutive value, ... where M cycles (M*N samples) have been accumulated. When the angle exceeds LIMIT1, the frequency deviation [delta*f] is computed at step **112**. However, to reduce the effect of transients on the frequency estimate, the frequency deviations are limited to +/-5 Hz at step 116 if [delta*f] exceeds 5 Hz as determined at step **114**. The sampling interval [delta*t] is then adjusted to obtain N samples per cycle at the new frequency at step **118** and the new phasor estimate becomes the reference phasor.
>
> *Hart*, col. 4, lines 24-49.

Applicant respectfully asserts that the foregoing passage does not teach or suggest capturing teach ensembles of data samples defined by successive resets of a cyclic counter, as required by claim 1. If the Examiner is relying on "common knowledge" or "well known" art in support of his rationale for combining the references, the Examiner is requested to produce a reference in support of his position pursuant to M.P.E.P. § 2144.03. Accordingly, Applicant respectfully requests that this rejection be withdrawn, or to the extent the rejection

is continued by the Examiner, that the Examiner provide support for such a rejection by reference to the art.

Claims 11, 15, 18, and 19, although indicated as rejected under 35 U.S.C. § 103(a), are not specifically addressed by the Examiner. Office Action, pages 3-4. Applicant respectfully points out that the rejection of claims 11, 15, 18, and 19 does not comport with Office policy because the Examiner has not "clearly articulate[d] any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise respond completely at the earliest opportunity." M.P.E.P. § 706. Therefore, Applicant respectfully requests that the Examiner set forth the specific grounds for rejection with respect to claims 11, 15, 18, and 19, so that that Applicant may have a full and fair opportunity to explore the patentability of these claims. *See* M.P.E.P. § 706.07.

IV.   Rejections Under § 103(a) over *Hart* in view of *Poimboeuf*

Claims 3-5, 7, 8, 12-14, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hart* in view of *Poimboeuf*.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the references' teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See M.P.E.P. § 2143. Applicant respectfully asserts that the rejection does not satisfy the basic criteria.

A.   Lack of Motivation

Claims 3-5, 7, 8, 12-14, and 20 are allowable because there is no suggestion or motivation in *Hart* or *Poimboeuf* to combine the clock synthesizer described in *Poimboeuf* with the generator protection system of *Hart*. The Examiner states that "[I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hart techinque [sic] to include the additional devices as taught by Poimboeuf at al to operate the processing signal more accurate [sic]." Office Action, pages 4-5. However, there is no indication of a need for more accurate signal processing in *Hart*. The mere fact that

references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

In addition, the language of the recited motivation is circular in nature, stating that it is obvious to make the combination because it is obvious to achieve the result. Such language is merely a statement that the reference can be modified and does not state any desirability for making the modification. Neither the prior art nor the knowledge available to a person of ordinary skill in the art suggest the desirability of the combination, and Applicants asserts that there is no suggestion or motivation to combine *Poimboeuf* with *Hart*. Applicant respectfully asserts that, for the above reasons, claims 3-5, 7, 8, 12-14, and 20 are patentable over the 35 U.S.C. § 103(a) rejection of record.

B.   Lack of All Claimed Limitations

1.   Claims 3-5, 7, and 8

As noted above, neither *Hart* nor *Poimboeuf* teach or suggest, at least, "capturing ensembles of data samples of said signal that are respectively defined by successive resets of said cyclic counter," as required by claim 1. Dependent claims 3-5, 7, and 8 depend from claim 1, and thus inherit all the limitations of that independent claim. Consequently, the combination of *Hart* and *Poimboeuf* also fails to teach or suggest all of the limitations of dependent claims 3-5, 7, and 8. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of record with respect to claims 3-5, 7, and 8 be withdrawn.

2.   Claims 12-14

As noted above, neither *Hart* nor *Poimboeuf* teach or suggest, at least, "sample capture circuitry ... operable to output time aligned ensembles of captured samples that are defined by respective resets of said cyclic counter logic," as required by claim 11. Dependent claims 12-14 depend from claim 11, and thus inherit all the limitations of that independent claim. Consequently, the combination of *Hart* and *Poimboeuf* also fails to teach or suggest all of the limitations of dependent claims 12-14. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of record with respect to claims 12-14 be withdrawn.

3.   Claim 20

As noted above, neither *Hart* nor *Poimboeuf* teach or suggest, at least, "means for outputting time aligned ensembles of samples defined by respective resets of said means for cyclically counting," as required by claim 18. Dependent claim 20 depends from claim 18, and thus inherit all the limitations of that independent claim. Consequently, the combination of *Hart* and *Poimboeuf* also fails to teach or suggest all of the limitations of dependent claim 20. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of record with respect to claim 20 be withdrawn.

V.   Conclusion

In view of the above remarks, Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-1078, under Order No. 10031555-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Label No. EV482709126US in an envelope addressed to: M/S Amendment, Commissioner for Patents, Alexandria, VA 22313.

Date of Deposit: September 13, 2005

Typed Name: Elise Perkins

Signature: _____

Respectfully submitted,

By: _____
Michael A. Papalas
Attorney/Agent for Applicant(s)
Reg. No. 40,381
Date: September 13, 2005
Telephone No. (214) 855-8186